IN THE CLAIMS

Please amend claim 4 as indicated below.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 2 (previously presented) A semiconductor device including a core and a periphery, the semiconductor device comprising:

a plurality of core gate stacks in the core, each of the plurality of core gate stacks including a first polysilicon gate and a WSi layer above the first polysilicon gate, wherein each of the plurality of core gate stacks includes an edge;

a plurality of core spacers, each of the plurality of core spacers residing along an edge of the plurality core gate stacks;

a plurality of sources in the core, the plurality of sources residing between a portion of the plurality of core gate stacks; and

a plurality of periphery gate stacks in the periphery, each of the plurality of periphery gate stacks including a second polysilicon gate and a CoSi layer on the second polysilicon gate.

Claim 3 (previously presented) The semiconductor device of claim 2 wherein each of the plurality of periphery gate stacks includes an edge, the semiconductor device further comprising:

a plurality of periphery spacers, each of the plurality of periphery spacers residing along an edge of the plurality periphery gate stacks.

Claim 4 (currently amended) ~~The semiconductor device of claim 2~~ A semiconductor device including a core and a periphery, the semiconductor device comprising:

a plurality of core gate stacks in the core, each of the plurality of core gate stacks including a first polysilicon gate and a WSi layer above the first polysilicon gate, wherein each of the plurality of core gate stacks includes an edge;

a plurality of core spacers, each of the plurality of core spacers residing along an edge of the plurality core gate stacks;

a plurality of sources in the core, the plurality of sources residing between a portion of the plurality of core gate stacks; and

a plurality of periphery gate stacks in the periphery, each of the plurality of periphery gate stacks including a second polysilicon gate and a CoSi layer on the second polysilicon gate;

wherein each of the plurality of core gate stacks includes the first polysilicon gate, the WSi layer above the first polysilicon gate, a layer of polysilicon above the WSi layer and a capping layer above the layer of polysilicon.

Claim 5 (original) The semiconductor device of claim 4 wherein the capping layer is a SiN layer.

Claim 6 (original) The semiconductor device of claim 4 wherein the capping layer is a SiON layer.

Claim 16 (previously presented) A semiconductor device comprising:

a plurality of core gate stacks in a core, wherein each of said plurality of core gate stacks comprises a first polysilicon gate and a WSi layer above said first polysilicon gate and a polysilicon capping layer above said WSi layer and an additional capping layer above said polysilicon capping layer;

a plurality of sources in said core, wherein said plurality of sources resides between a portion of said plurality of core gate stacks; and

a plurality of periphery gate stacks in a periphery, wherein each of said plurality of periphery gate stacks comprises a second polysilicon gate and a CoSi layer above said second polysilicon gate.

Claim 17 (previously presented) The semiconductor device as recited in claim 16, wherein said additional capping layer functions as an antireflective layer.

Claim 18 (previously presented) The semiconductor device as recited in claim 16, wherein said additional capping layer is a SiN layer.

Claim 19 (previously presented) The semiconductor device as recited in claim 16, wherein said additional capping layer is a SiON layer.